Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB; PLUR=YES; OP=OR			
L19	L18 and l2	14	L19
L18	L17 and l15	108	L18
L17	redundan$ same l1	5454	L17
L16	L15 and l11	0	L16
L15	L14 same error	3878	L15
L14	L12 same correct$	9927	L14
L13	L12 and l11	182	L13
L12	(chang$ or revers$) same bit	103849	L12
L11	L3 same fuse	698	L11
L10	L3 and l8	0	L10
L9	L8 same error	10	L9
L8	chang$ near3 polarity near2 bit	180	L8
L7	L4 same correct$	0	L7
L6	L3 and l4	0	L6
L5	L4 same error	0	L5
L4	revers$ near2 sense near2 bit	43	L4
L3	L2 same l1	1944	L3
L2	defective near2 cell	6475	L2
L1	address same memory	190804	L1

END OF SEARCH HISTORY

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L9: Entry 3 of 10 File: USPT Jun 30, 1998

DOCUMENT-IDENTIFIER: US 5774481 A
TITLE: Reduced gate error detection and correction circuit

Brief Summary Text (5):
To ensure the integrity of data stored in a data processing system and transmitted between various parts of the system, various error detection and correction schemes have been employed. Known schemes, such as the Hamming code, allow for double error detection and single error correction. Typically, before a data word is stored in a memory, check bits are generated over the data bits and stored with the data word. When the data word is retrieved from memory, a check is made over the data and the check bits to detect and, if necessary, to correct identifiable bits. In checking the data word and error bits received from memory, a syndrome is generated for each parity group of a multiple byte data word. A matrix, referred to as an H-matrix, may be generated which defines all of the syndromes for which a single error is correctable and which identifies each bit position of the data word which is correctable. When a syndrome is generated which matches the data in one of the columns of the matrix, the bit to be corrected is identified from the matrix and the polarity of the identified bit is changed to correct the data error. Additional tests need to be made to determine whether there are uncorrectable errors. When dealing with 64-bit data words, the H-matrix has 64 columns, plus columns for check bits. The number of syndromes which may be generated and which do not fall within the matrix are considerably larger than the correctable-error syndromes included in the matrix. A typical error correction scheme using 8-bit syndromes for 64 bits of data, and requiring single error correction and double error detection, will have 256 possible syndromes and 72 syndromes associated with correctable errors. The detection of the presence of a correctable error and the presence of uncorrectable errors requires large amounts of detection circuitry adding considerably to the cost of the system.

Detailed Description Text (2):
FIG. 1 is a block diagram representation of error detection and correction circuitry incorporating principles of the invention. FIG. 1 includes a data input register 110 in which data and an error control code (ECC) are received from a memory 101 in a standard memory read operation. For the purposes of error detection and correction, a syndrome is generated by means of a well known syndrome generator 112. The output of the syndrome generator 112 is connected via a bus 115 to an uncorrectable-error (UE) detection circuit 116, a zero detect circuit 117, a correctable-error (CE) detection circuit 118, and a flip controller 120. The zero detect circuit 117 provides an output when syndrome consists of all zeroes, which has been defined in the present system as a no-error condition. The outputs of the zero detect circuit 117, the UE detect circuit 116, and the CE detect circuit 118 may be tested for orthogonality, i.e. that one and only one of these three circuits generates an output signal for each tested syndrome, in orthoganality detect circuit 119. Circuit 119 may be standard logic circuit generating an error output when if the orthogonality condition is not satisfied. The data input register 110 also is connected to data flip logic 123. The flip controller 120 decodes the syndrome obtained from the bus 115 and generates an appropriate output when the syndrome indicates a single, correctable error in a bit location of the data in memory register 110. The output of flip controller 120 is used to change the polarity of a specific bit identified by the syndrome in order to correct the data in the data flip logic 123. The corrected output of flip logic 123 is gated to the data output register 122.

Detailed Description Text (10):
The flip logic in 120 in FIG. 1 operates to "flip" or change the polarity of a particular bit found in error. The flip logic decodes the syndrome and if a particular one of the syndromes in the H-matrix of Table A is found, an output will be generated by the flip logic circuit 120 to flip the particular bit position corresponding to the

detected syndrome. The output of the flip logic 120 is used to flip the selected data bit in the data flip logic 123, which corresponds to the data received from the data register 110. The contents of the data flip logic 123 is subsequently stored in the data output register 122. The parity bit may be flipped by means of the flip parity circuit 124 from the flip logic 120 if it appears that the parity bit is in error.

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L19: Entry 8 of 14 File: USPT Aug 28, 2001

DOCUMENT-IDENTIFIER: US 6282689 B1
**** See image for Certificate of Correction ****
TITLE: Error correction chip for memory applications

Abstract Text (1):
A memory module, such as a SIMM or DIMM, is provided which incorporates error correction circuitry. The error correction circuitry identifies and corrects errors in communications between the memory module and an external processor. A reliable data processing system is also provided, incorporating the memory module comprising the error correction circuitry with a processor. The yield of manufactured chips is increased by presorting the memory chips which make up the memory module, such that a chip with one or more defective cells may be included in a memory module so long as no other chip has defective cells at the same location.

Brief Summary Text (4):
Systems for storing and recalling information have been developed over the years in conjunction with the advances in computing technology. One of the primary considerations in architecting these memory systems is the ability to accurately read the incoming information and reproduce it correctly when writing it out again. Such electronically-represented information is comprised of a series of bits, each bit having a total of two possible states. It is recognized that a change in the value of a single bit can greatly affect the outcome of a mathematical operation or the meaning of the recorded information. Completely error-free transmission is as-of-yet unattainable. Data errors introduced during transmission, however, can be greatly reduced by the use of parity bits. Simply described, additional bits are added to the string of data bits in a predetermined pattern such that if an error is later introduced the error is detectable and often able to be corrected by logic at the receiving end. One of the better-known codes employed to provide such an error management system was developed by R. W. Hamming and is referred to as Hamming code. In its simplest form a message is divided into fixed-length blocks of bits where some of the bits are data bits and the rest of the bits are check bits which are set according to the Hamming code pattern. The ratio of data bits to check bits is such that in any one block any double-bit error can be detected and all single-bit errors are corrected.

Brief Summary Text (11):
Another feature provided by the present invention is chip yield enhancement. In one embodiment of the present invention, the memory devices are sorted before they are included in the memory module, such that there is zero correlation of failing bits among the memories in any one memory module. Also provided is a method of populating a memory module, the memory module having a plurality of independently addressable memory devices and error detection circuitry. The method comprises the steps of testing individual memories to determine locations of defective cells, selecting a plurality of the individual memories such that there is no coincidence of the locations of defective cells among the selected plurality of individual memories, and mounting the selected plurality of individual memories on the memory module such that the error detection circuitry is electrically located between the plurality of memories and an external processor. By this method and system less-than-perfect memory devices are productively used rather than having to be discarded.

Detailed Description Text (6):
In the conventional memory module of FIG. 2, in order to ensure that a functional memory cell is being accessed, the architecture must include either redundancy or error management processing external to the memory module. This adds expense in both processing time and manufacturing costs. The need for a means to verify and correct communications with memory devices results from the unavoidable fact that memory devices will have defects. Memory devices are typically manufactured with redundant

circuits which can be programmed to replace defective cells after exhaustive testing is conducted to identify which cells on a memory chip has failed. The redundant cells are activated through the use of fuse and anti-fuse circuits. It will be appreciated that as the memory cell density is increased, more redundant cells are needed. As known to those skilled in the art, an anti-fuse is a normally open circuit which is shorted when programmed. A popular type of anti-fuse is a capacitor fabricated similar to a DRAM memory cell. The current oxide-nitride-oxide (ONO) dielectric used in DRAM memory cell capacitors is ideal for anti-fuse fabrication. Anti-fuse fabrication is complicated, however, as a result the trend toward manufacturing DRAMs with a barium-strontium-titanium (BST) dielectric between the memory cell capacitor plates rather than the conventional ONO dielectric.

Detailed Description Text (8):
The present invention effectively increases the manufacturing yield of the memory devices by allowing the use of less-than-perfect chips. That is, the error correction circuit allows the use of normally defective memory devices. This is accomplished by pre-sorting the memory chips before installing them on a memory module such that there is zero correlation of failing cells among the memories of a memory module. During testing redundant cells can be used to correct defective memory cells. However, if there are more defects than available redundant cells the address locations of remaining defective cells are recorded. The addresses of failing cells on each chip can then be compared to find the best groupings for a memory module 200. As a result, memory devices which would normally be considered defective can be used.

CLAIMS:

11. A method of constructing a memory module from a plurality of memory devices, the method comprising:

using redundant cells in the plurality of memory devices to correct memory defects on the plurality of memory devices;

recording the addresses of remaining defective cells on the memory device when all redundant cells in a memory device are used; and

grouping for zero correlation the remaining defective memory cells in the memory devices.

12. A method of constructing a memory module as described in claim 11, wherein grouping for zero correlation further comprises:

comparing the addresses of the defective cells on each memory device to find the best grouping for a memory device.

18. A method of constructing a memory device, the method comprising:

recording the addresses of failing memory cells on a plurality of normally defective memory modules; and

grouping for zero correlation the remaining defective memory cells in the memory devices.

19. A method of constructing a memory device as described in claim 18, wherein grouping the remaining defective memory cells further comprises:

sorting the normally defective memory modules such that there is zero correlation of failing memory cells on the normally defective memory modules.

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